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(211.004-US)

In re Application of: **FERRANT ET AL.**

U.S. Application Serial No: **10/840,009**

U.S. Filing Date: **MAY 6, 2004**

Title: **SEMICONDUCTOR MEMORY DEVICE AND METHOD OF OPERATING SAME**

Group Art Unit: **2818**

Examiner:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on August 11, 2004
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(person signing this certificate)
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SECOND INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Submitted herewith are seven (7) sheets of modified Form PTO-1449. A copy of each document identified on the Form PTO-1449 is also submitted.

It is respectfully requested that the Examiner make his/her consideration of these documents formally of record with the initial Office Action.

Respectfully submitted,

Date: August 11, 2004

Neil A. Steinberg
Reg. No. 34,735
650-968-8079

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Sheet 1 of 7

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. 211.004-US	SERIAL NUMBER 10/840,009
	APPLICANT(S) Ferrant et al.	
	FILING DATE May 6, 2004	GROUP ART UNIT 2813

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

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	"A Capacitorless Double-Gate DRAM Cell", Kuo et al., IEEE Electron Device Letters, Vol. 23, No. 6, June 2002, pp.345-347
	"A Capacitorless Double-Gate DRAM Cell for High Density Applications", Kuo et al., IEEE IEDM, 2002, pp.843-946
	"The Multi-Stable Behaviour of SOI-NMOS Transistors at Low Temperatures", Tack et al., Proc. 1988 SOS/SOI Technology Workshop (Sea Palms Resort, St. Simons Island, GA, Oct. 1988), p.78
	"The Multistable Charge-Controlled Memory Effect in SOI MOS Transistors at Low Temperatures", Tack et al., IEEE Transactions on Electron Devices, Vol. 37, No. 5, May 1990, pp.1373-1382
	"Mechanisums of Charge Modulation in the Floating Body of Triple-Well nMOSFET Capacitor-less DRAMs", Villaret et al., Proceedings of the INFOS 2003, Insulating Films on Semiconductors, 13th Bi-annual Conference, June 18-20, 2003, Barcelona (Spain), (4 pages)
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	"High-Endurance Ultra-Thin Tunnel Oxide in MONOS Device Structure for Dynamic Memory Application", Wann et al., IEEE Electron Device Letters, Vol. 16, No. 11, November 1995, pp.491-493
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	"A Simple 1-Transistor Capacitor-Less Memory Cell for High Performance Embedded DRAMs", Fazan et al., IEEE 2002 Custom Integrated Circuits Conference, June 2002, pp.99-102
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	"Capacitor-Less 1-Transistor DRAM", Fazan et al., 2002 IEEE International SOI Conference, Oct. 2002, pp.10-13
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	"Triple-Wel nMOSFET Evaluated as a Capecitor-Less DRAM Cell for Nanoscale Low-Cost & High Density Applications", Villaret et al., Handout at Proceedings of 2003 Silicon Nanoelectronics Workshop, June 8-9, 2003, Kyoto, Japan (2 pages)
	"Mechanisms of Charge Modulation in the Floating Body of Triple-Well NMOSFET Capacitor-less DRAMs", Villaret et al., Handout at Proceedings of INFOS 2003, June 18-20, 2003, Barcelona, Spain (2 pages)
	"Embedded DRAM Process Technology", M. Yamawaki, Proceedings of the Symposium on Semiconductors and Integrated Circuits Technology, 1998, Vol. 55, pp.38-43
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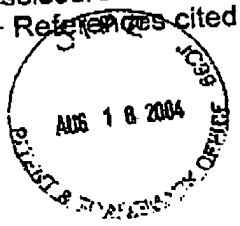
SERIAL NO.: **10/840,009**

TITLE: **Semiconductor Memory Device and Method of Operating Same**

RECEIPT OF THE FOLLOWING PAPERS IS ACKNOWLEDGED

1. Second Information Disclosure Statement (1 page + Modified Form-PTO-1449 (7 pages) + References cited therein)



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	APPLICANT(S) Ferrant et al.	
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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
	EP 0 366 882 B1	5/1995	European				
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	EP 0 354 348 A2	2/1990	European				
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	EP 1 233 454 A2	8/2002	European				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(211.004-US)

APPLICANT: Ferrant et al. Filed: May 6, 2004

SERIAL NO.: 10/840,009

TITLE: Semiconductor Memory Device and Method of Operating Same

RECEIPT OF THE FOLLOWING PAPERS IS ACKNOWLEDGED

1. Fourth Information Disclosure Statement (1 page + Modified Form-PTO-1449 (5 pages) + References cited therein)

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